IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A signal level detector comprising:

a first voltage/current conversion circuit which outputs a first current which depends on a voltage amplitude of an inputted signal;

a second voltage/current conversion circuit which outputs a second current which depends on an inputted reference voltage signal; and

~~a comparison~~ a control circuit ~~which compares~~ having a control input configured to receive a first signal from the first voltage/current conversion circuit indicative of the first current ~~with~~ and a second signal from the second voltage/current conversion circuit indicative of the second current and ~~outputs~~ an output stage configured to provide a control signal based on ~~a comparison result~~ the first and second signals received at the control input, the output stage including a common gate connected to the control input,

wherein the first voltage/current conversion circuit outputs the first current which depends on a square of a voltage amplitude of the inputted signal, and the second voltage/current conversion circuit outputs the second current which depends on a square of an amplitude of the inputted reference voltage signal.

Claim 2 (Original): The signal level detector according to claim 1, wherein the inputted signal is a differential signal, and the inputted reference voltage signal includes two reference voltages.

Claim 3 (Canceled).

Claim 4 (Original): The signal level detector according to claim 1, further comprising a first capacitance element and a second capacitance element respectively connected between an output terminal of the first voltage/current conversion circuit and a ground potential and

between an output terminal of the second voltage/current conversion circuit and the ground potential.

Claim 5 (Original): The signal level detector according to claim 1, further comprising a first resistance element and a second resistance element, respectively connected between an output terminal of the first voltage/current conversion circuit and a ground potential and between an output terminal of the second voltage/current conversion circuit and the ground potential.

Claim 6 (Currently Amended): The signal level detector according to claim 1, wherein the ~~comparison circuit~~ control input includes[[,]] ~~as an output end~~[[,]] a connection node directly connecting between an output terminal of the first voltage/current conversion circuit and an output terminal of the second voltage/current conversion circuit, and a capacitor connected between the connection node and a ground potential.

Claim 7 (Currently Amended): The signal level detector according to claim 6, wherein the first current is a charging current which flows out from the output terminal of the first voltage/current conversion circuit, and the second current is a discharging current which flows into the output terminal of the second voltage/current conversion circuit.

Claim 8 (Currently Amended): The signal level detector according to claim 6, wherein the first current is a discharging current which flows into the output terminal of the first voltage/current conversion circuit, and the second current is a charging current which flows out from the output terminal of the second voltage/current conversion circuit.

Claim 9 (Currently Amended): A signal level detector comprising:

a first squaring circuit to which a first voltage signal is inputted and which outputs a first current including a square component of an input amplitude of the first voltage signal;

a second squaring circuit to which a reference voltage signal is inputted and which outputs a second current including a square component of an amplitude of the reference voltage signal; and

a control circuit including a comparison circuit which compares a first output voltage which is in proportion to the first current with a second output voltage which is in proportion to the second current, the comparison circuit being configured to provide a comparison output ~~outputs a control~~ signal,

wherein the control circuit further includes a common gate connected to receive the comparison output signal of the comparator, and

wherein the control circuit outputs a control signal used to detect the first voltage signal based on ~~a~~ the comparison ~~result~~ output signal supplied to the common gate.

Claim 10 (Original): The signal level detector according to claim 9, wherein the first voltage signal is a differential signal, and the reference voltage signal includes two reference voltages.

Claim 11 (Original): The signal level detector according to claim 9, further comprising a first capacitance element and a second capacitance element respectively connected between an output terminal of the first squaring circuit and a ground potential and between an output terminal of the second squaring circuit and the ground potential.

Claim 12 (Original): The signal level detector according to claim 9, further comprising a first resistance element and a second resistance element respectively connected between an output terminal of the first squaring circuit and a ground potential and an output terminal of the second squaring circuit and the ground potential.

Claim 13 (Currently Amended): The signal level detector according to claim 9, wherein the comparison circuit includes[[,]] ~~as an output end~~[[,]] a connection node at an output of the comparison circuit providing the comparison output signal to the common gate

~~directly connecting between an output terminal of the first squaring circuit and an output terminal of the second squaring circuit~~ and a capacitor connected between the connection node and a ground potential.

Claim 14 (Currently Amended): The signal level detector according to claim 13, wherein the first current is a charging current which ~~flows out from the output terminal~~ charges the capacitor, and the second current is a discharging current which ~~flows into the output terminal~~ charges the capacitor.

Claim 15 (Currently Amended): The signal level detector according to claim 13, wherein the first current is a discharging current which ~~flows into the output terminal~~ discharges from the capacitor, and the second current is a charging current which ~~flows out from the output terminal~~ charges the capacitor.

Claim 16 (Currently Amended): An amplification factor control system comprising:

an amplification circuit ~~which~~ configured to output an output signal by amplifying a reception signal inputted thereto with an amplification factor according to a control signal; and

a signal level detector to which the output signal is inputted and which includes a first voltage/current conversion circuit which outputs a first current which depends on a voltage amplitude of the output signal, a second voltage/current conversion circuit which outputs a second current which depends on a reference voltage signal inputted thereto, and ~~a comparison~~ a control circuit ~~which compares~~ having a control input configured to receive a first signal indicative of the first current ~~with~~ and a second signal indicative of the second current and ~~outputs~~ an output stage configured to provide the control signal based on ~~a comparison result~~ the first and second signals received at the control input, the output stage includes a common gate configured to be connected to the control input.

Claim 17 (Previously Amended): The amplification factor control system according to claim 16, wherein the first voltage/ current conversion circuit outputs the first current which depends on a square of a voltage amplitude of the output signal, and the second voltage/current conversion circuit outputs the second current which depends on a square of an amplitude of the reference voltage signal.

Claim 18 (Previously Amended): The amplification factor control system according to claim 16, wherein the control signal increases with increase in the output signal from the amplification circuit.

Claim 19 (Previously Amended): The amplification factor control system according to claim 16, wherein the control signal decreases with decrease in the output signal from the amplification circuit.

Claim 20 (Original): The amplification factor control system according to claim 16, further comprising a capacitance element connected between a terminal to which the control signal is applied and a ground potential.

Claim 21 (Currently Amended): A signal level detector comprising:

a first voltage/current conversion circuit which outputs a first current which depends on a voltage amplitude of an inputted signal, the inputted signal being a differential signal;

a second voltage/current conversion circuit which outputs a second current which depends on an inputted reference voltage signal, the inputted reference voltage signal including two reference voltages; and

~~a comparison~~ a control circuit ~~which compares~~ having a control input configured to receive a first signal indicative of the first current ~~with~~ and a second signall indicative of the second current and ~~outputs~~ an output stage configured to provide ~~the~~ a control signal based on ~~a comparison result~~ the first and second signals received at the control input, the output stage including a common gate configured to be connected to the control input.

Claim 22 (New): The signal level detector according to Claim 1, wherein the output stage includes:

a first constant current source an end of which is connected to a power supply;

a pMOSFET having a first source, a first drain and a first gate, the first source being connected to the other end of the first constant current source;

an nMOSFET having a second source, a second drain and a second gate, the second drain being connected to the first drain to output the control signal, the second gate being connected to the first gate to form the common gate; and

a second constant current source an end of which is connected to the second source and the other end of which is connected to a ground potential.

Claim 23 (New): The signal level detector according to Claim 9, wherein the output stage includes:

a first constant current source an end of which is connected to a power supply;

a pMOSFET having a first source, a first drain and a first gate, the first source being connected to the other end of the first constant current source;

an nMOSFET having a second source, a second drain and a second gate, the second drain being connected to the first drain to output the control signal, the second gate being connected to the first gate to form the common gate; and

a second constant current source an end of which is connected to the second source and the other end of which is connected to a ground potential.

Claim 24 (New): The signal level detector according to Claim 16, wherein the output stage includes:

a first constant current source an end of which is connected to a power supply;

a pMOSFET having a first source, a first drain and a first gate, the first source being connected to the other end of the first constant current source;

an nMOSFET having a second source, a second drain and a second gate, the second drain being connected to the first drain to output the control signal, the second gate being connected to the first gate to form the common gate; and

a second constant current source an end of which is connected to the second source and the other end of which is connected to a ground potential.

Claim 25 (New): The signal level detector according to Claim 21, wherein the output stage includes:

a first constant current source an end of which is connected to a power supply;

a pMOSFET having a first source, a first drain and a first gate, the first source being connected to the other end of the first constant current source;

an nMOSFET having a second source, a second drain and a second gate, the second drain being connected to the first drain to output the control signal, the second gate being connected to the first gate to make the common gate; and

a second constant current source an end of which is connected to the second source, and the other end of which is connected to a ground potential.